Time-to-Digital Converter
Quad-Channel USB3.0-TDC 04R
(Release 042, 043, 044, 052, 053)

Manual

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User Manual for the
Quad Channel USB3.0-TDC 04R
Releases: 042, 043, 044, 052, 053
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1 Table of Contents


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2 Introduction

2.1 General Information

This manual is intended to provide an overview of the Quad-Channel USB3.0-TDC 04R in Release 042, 043, 044, 052 and 053 as part of a delayline detector package. It is divided into 7 chapters. The chapter "Introduction" contains a brief description of the device. The chapter "Installation" refers to installation and cabling. The other chapters contain amongst others technical details and the description of the device layout.

2.2 Safety Instructions

Please read this manual carefully before performing any electrical or electronic operations and strictly follow the safety rules given within this manual. Surface Concept declines all responsibility for damages or injuries caused by an improper use of the module due to negligence on behalf of the User.

The following symbols may appear throughout the manual:

The "note symbol" marks text passages, which contain important information/hints about the operation of the detector. Follow these information to ensure a proper functioning of the detector.

The "caution symbol" marks warnings, which are given to prevent an accidental damaging of the detector or the readout system. Do NOT ignore these warnings and follow them strictly. Otherwise no guarantee is given for arose damages.

The "high voltage symbol" marks warnings, given in conjunction with the description of the operation/use of high voltage supplies and/ or high voltage conducting parts. Hazardous voltages are present, which can cause serious or fatal injuries. Therefore only persons with the appropriate training are allowed to carry out the installation, adjustment and repair work.

2.3 General Overview

The Surface Concept Quad-Channel USB3.0-TDC 04R in Release 042 and 043 are the basic versions of the special Surface Concept Time-to-Digital Converters for the readout of the Surface Concept Delayline Detectors. They come in a 19“ rack mount housing (R042) or in a stand alone table top housing (R043).
The USB3.0-TDC 04R in Release 044 bases on the Release R042, but comes with additional inputs (like TAG IN, ADC IN) for an extended measurement functionality.
The USB3.0-TDC 04R in Release 052 also bases on the Release R042, but comes with an integrated 2 channel HV supply in addition for supplying the delayline detector, while the USB3.0-TDC 04R in Release 053 bases on the Release R052 but includes the additional inputs (like TAG IN, ADC IN) for an extended measurement functionality, comparable to the Release R044.

The two channel HV supply as part of the TDC R052 and R053 is especially laid out for the operation of Surface Concept Delayline Detectors. It holds four HV connectors. Up to three of those are used for high voltage outputs to connect to the corresponding high voltage inputs of the delayline detectors and one high voltage input for an external reference voltage.
In the standard connection layout R052 and R053 provide positive voltages for the supply of the MCP stack and the detector anode. The output voltages are referred to an external reference potential, which can be connected in addition.
The maximum output voltage is higher than the normal operation voltage of a delayline detector. Therefore please check the specification sheet of your delayline detector for the correct and the maximum operation voltage.

The device can produce lethal high voltages of up to several kV. Hazardous voltages are present, therefore only persons with the appropriate training are allowed to carry out the installation, adjustment and repair work.

Do not open the power supply, while it is in operation. Hazardous voltages are present. In case that the device must be opened, turn off the device first AND pull out the power plug.

3 Installation

3.1 Initial Inspection

Visual inspection of the system is required to ensure that no damage has occurred during shipping. Should there be any signs of damage, please contact our provider immediately. Please check the delivery according to the packing list (see **Table 1a** and **Table 1b**) for completeness.

- Quad Channel USB3.0–TDC 04R (R042, R043, R044)
- 1x USB cable
- 1x power cable

Table 1a: Packing list for the TDC (R042, 043, 044)

- Quad Channel USB3.0–TDC 04R (R052, R053)
- 1x USB cable
- 3x SHV cables
- 1x SHV termination plug
- 1x BNC termination plug
- 1x power cable

Table 1b: Packing list for the TDC (R052, 053)

3.2 Cabling

The general connection scheme of the delayline detector including its readout package is shown in the corresponding delayline detector manual. A TDC specific connection scheme for the different TDC layouts are given in **Figure 1a - e**.

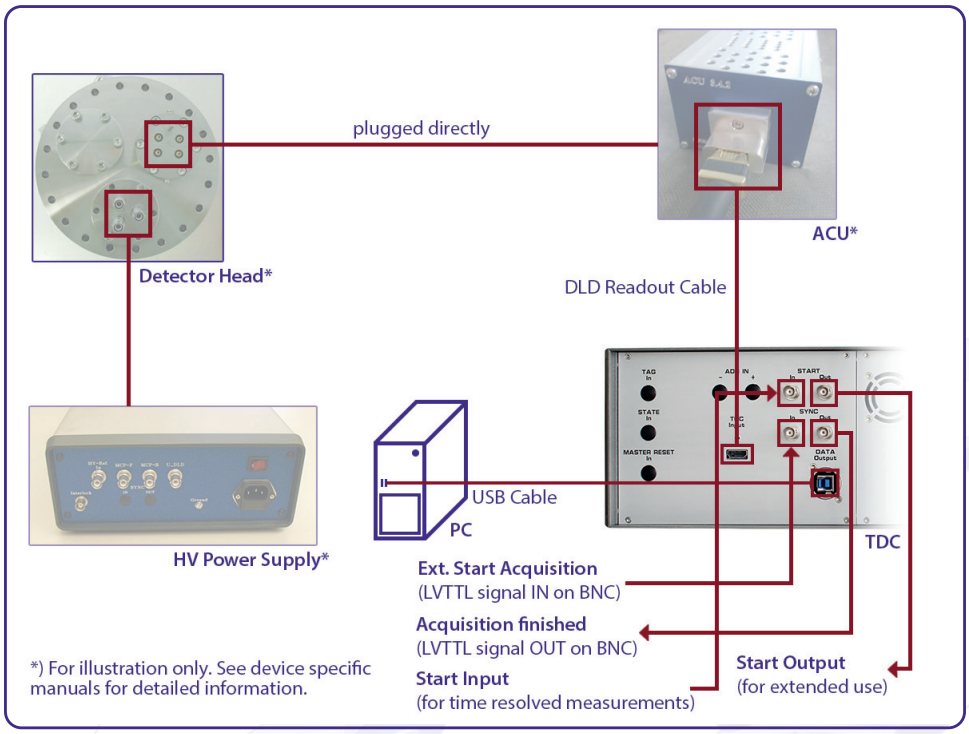

Figure 1a: Specific connection scheme of the Quad-Channel USB3.0-TDC R042 to a Surface Concept Delayline Detector.

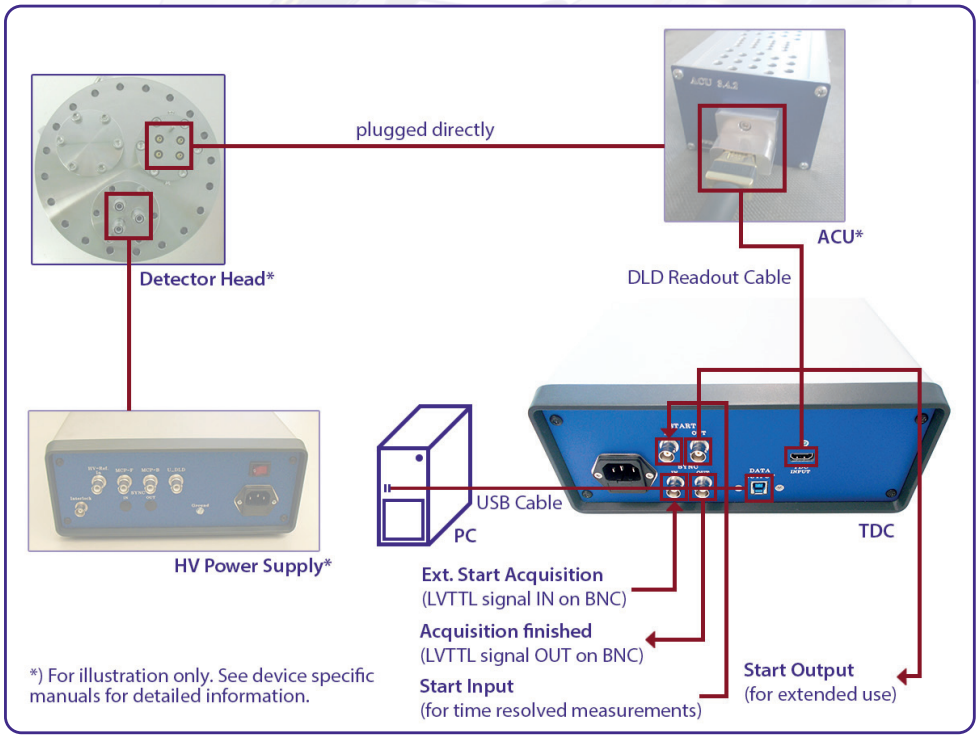

Figure 1b: Specific connection scheme of the Quad-Channel USB3.0-TDC R043 to a Surface Concept Delayline Detector.

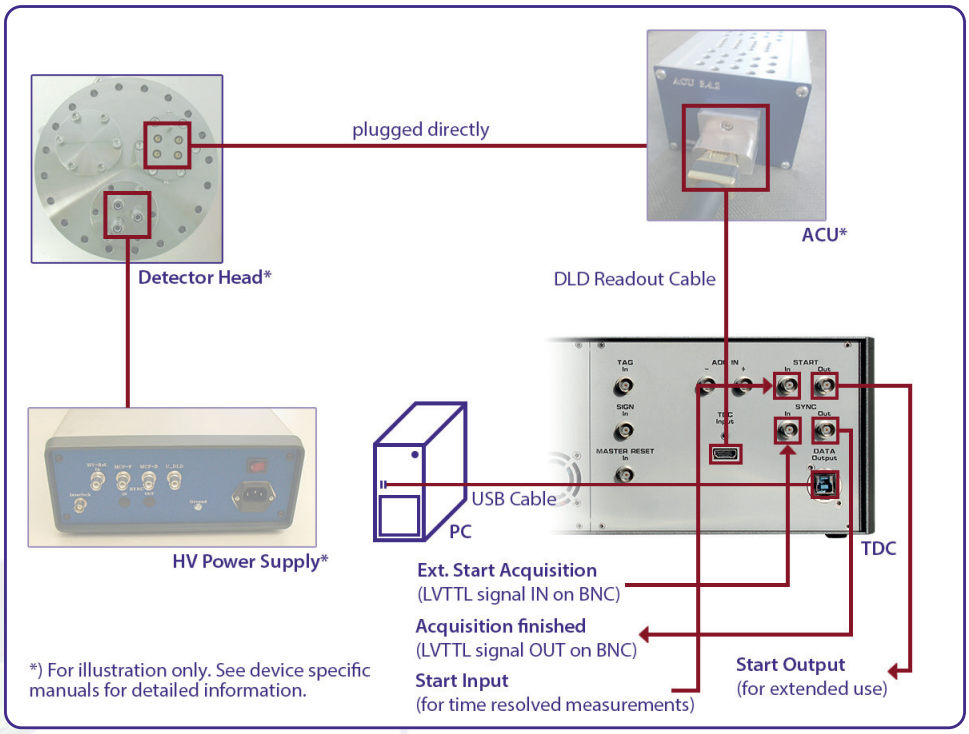

Figure 1c: Specific connection scheme of the Quad-Channel USB3.0-TDC R044 to a Surface Concept Delayline Detector.

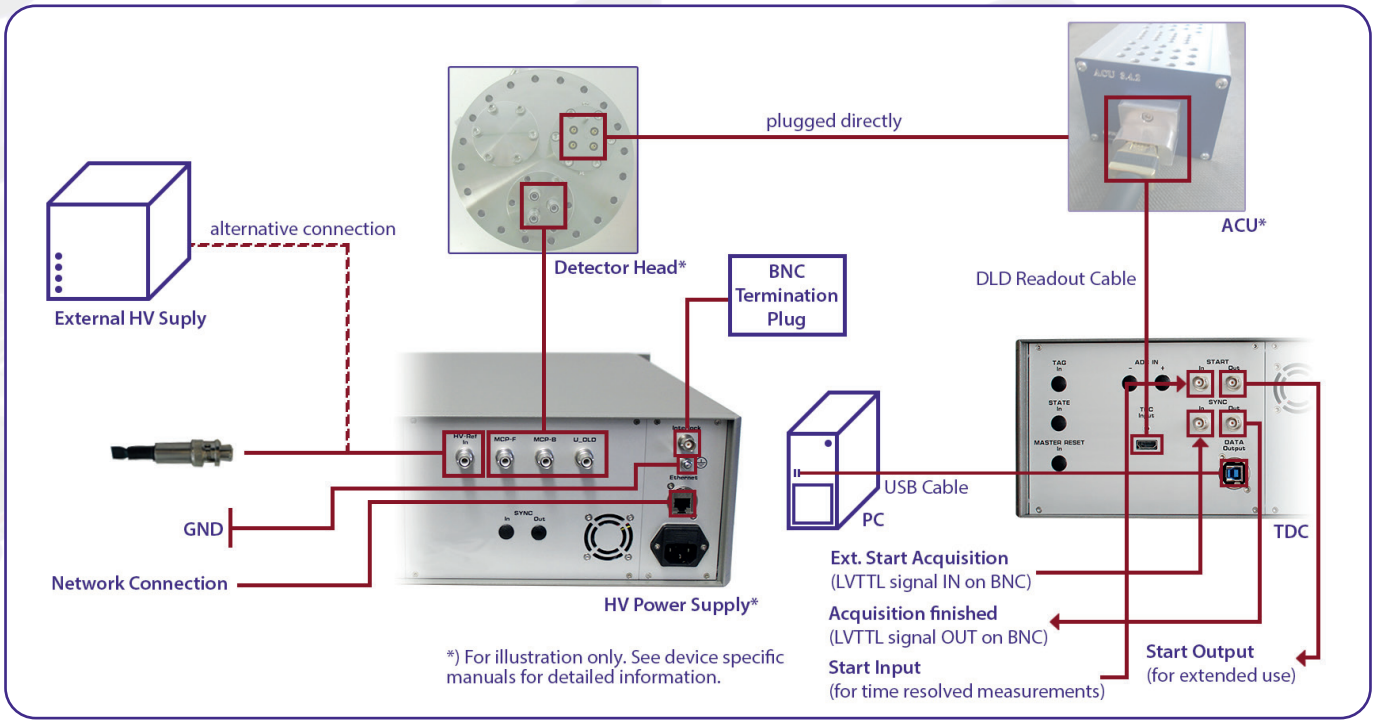

Figure 1d: Specific connection scheme of the Quad-Channel USB3.0-TDC R052 to a Surface Concept Delayline Detector.

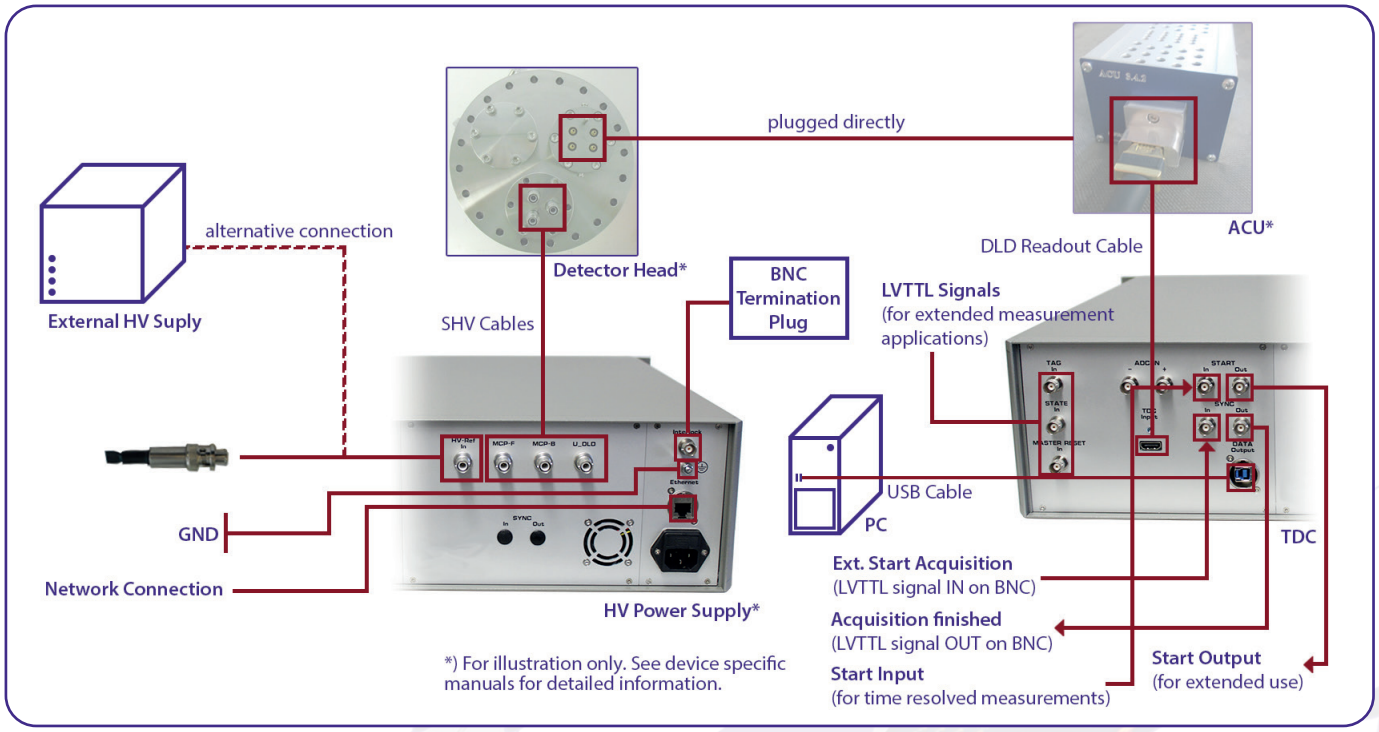

Figure 1e: Specific connection scheme of the Quad-Channel USB3.0-TDC R053 to a Surface Concept Delayline Detector.

For all release versions

- First, use the "Ground" connector (M4 screw) to ground the device.
- Use the DLD readout cable to connect the "Lines Out" socket on the front of the ACU with the "TDC Input" socket at the rear panel of the USB3.0-TDC. The readout cable holds strain-relief to fix the cable to the ACU as well as to the TDC.
- To perform time measurements with respect to an external clock, provide start pulses to the start input of the TDC. Use the BNC socket named "TTL Start" to apply LVTTL (low voltage TTL) signals (see **Chapter 4.3.2** for detailed information).
- Use the USB cable to connect the USB3.0-TDC to the PC. Do not use PC front panel USB connectors; they are often restricted in performance (see **Chapter 3.3** for further details)
- Connect the power cable to the main connector.
- Install the TDC device driver or software package prior to switching on the TDC.

For release versions R044, R053

- Use BNC cables to connect your additional signals to the additional inputs of the TDC (e.g. TAG IN).
- Please note that all additional inputs are internally 50Ohm terminated and are laid out for 50Ohm terminated LVTTL signal levels.

For release versions R052, R053

- High voltage output is provided to the SHV sockets named "MCP-B" and "U_DLD" .
- The socket named "MCP-F" connects the external reference voltage which is given to the device via the "HV Ref. In" input to the front side of the MCP stack.
- Use the HV cables to connect the HV outputs to the corresponding HV inputs of the delayline detector (see DLD manual for more details).
- Use the SHV termination plug to terminate the "HV Ref. In" input when not working with an external reference voltage.
- Check if the Interlock-Plug (BNC termination plug) is connected.

Note

In cases that no reference voltage is applied to the device, the termination plug must be used to ground the reference input of the high voltage modules. With a missing reference potential the high voltage modules do not providing any output voltage.

Finish the complete cabling before the TDC is turned on and the GUI software is started. Also, close the software and turn off the TDC before performing any changes to the cabling.
This applies especially to the connection and disconnection of the start input of the TDC. The start input of the TDC cannot handle pulses which are arriving in a time interval of smaller than 120ns, as they are produced by e.g. connecting to and disconnecting from the start input respectively.
If two subsequent pulses are applied to the start input of the TDC, the device will still deliver results, but these results will contain wrong timing information.

3.3 Software Installation, Requirements and Interface

All operation functions of the TDCs for data readout of the detector package are encapsulated in a dynamic linked library (scTDC1.dll). Data processing and presentation on the PC is realized by an end-user software (e.g. GUI). See the corresponding software manual for detailed information on the software package and the DLL interface.

The delivery package of the delayline detector includes a storage medium with hardware drivers and the GUI software. Connect the storage medium to your PC and install the software package as described in the Software Installation Manual.

Read-out of the TDC is done with a standard PC via USB3.0. For the PC the following minimum system requirements are highly recommended:

- Processor: Quad Core
- RAM: 4GB
- Windows 7 or higher
- USB (no front panel connector)

! Note

Depending on the specific PC system used for the TDC readout (mainly depending on the specific USB3.0 chip used on the PC motherboard), the use of USB3.0 can lead to instabilities in the data communication. For those cases we then recommend the use of USB2.0. The use of USB2.0 is always possible, but there might be limitations in the maximum count rates for certain detector types and/or detector operation modes.

4 TDC Layout

4.1 Schematic Description of the TDC Section

The USB3.0-TDC series combines the excellent performance of the GPX TDC chip with a high speed USB interface.

A field programmable gate array (FPGA) enables comfortable setups and a variable data stream handling from the TDC via USB.
The main delayline detector readout functionality is permanently programmed. A complex FIFO design makes data losses almost impossible. The user DLL controls the data handling and streaming for the user.

The following brief description about the internal structure of the measurement unit is only informative:

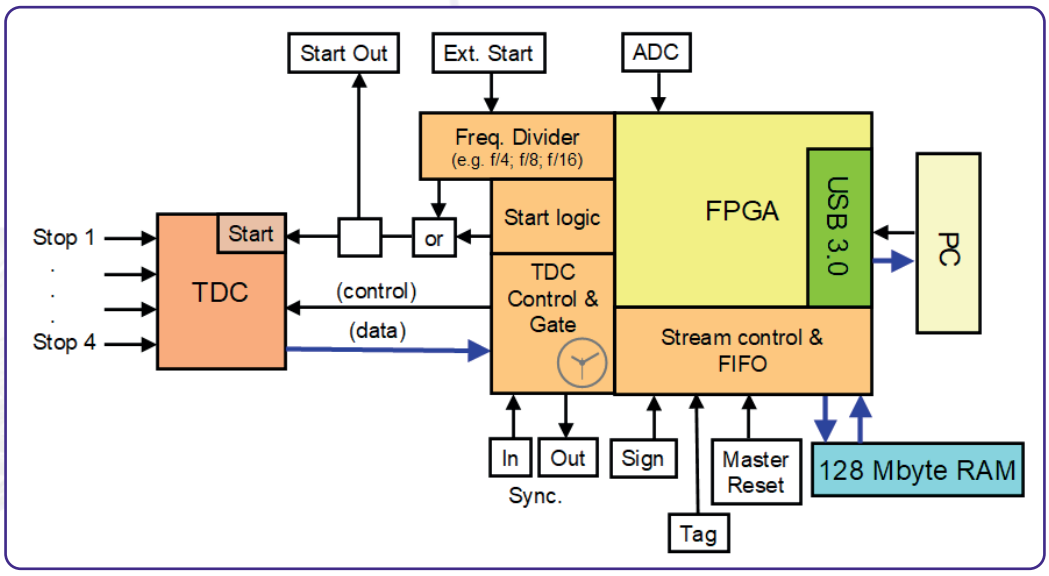

Figure 2: Schematic sketch of TDC functioning.

Arrival times of pulses at the stop inputs are measured by the TDC with respect to either an internal reference start signal, provided by the FPGA, or an external start signal. An internal electronics provide the TDC start signal to an additional BNC socket for further extended measurement use. The measurement dwell times for data from the TDC are settled within the FPGA by a quartz stabilized time gate in an interval from 1ms to 1193h.
A synchronization pulse can be fed directly into the FPGA (SYNC IN) controlling the acquisition process (synchronization to external processes, see **Chapter 4.3.4**). The FPGA also sends out a synchronization pulse for marking the end of an acquisition (SYNC OUT).

Additional inputs (e.g. TAG or ADC) are available (R044, R053) to feed in additional signals directly into the TDC data stream for extended measurement functionality.

The TDC data streaming can be performed with a specific pre-conditioning of the DLD data, which includes channel pairing, pair result arithmetics and many more. Communication to and from the PC is achieved via a USB interface. Data streaming via the USB interface is provided without losses using a large memory buffer within the device.

4.2 Schematic Description of the HVPS Section

Figure 3 shows the schematic layout of the HVPS section of the Quad Channel USB3.0-TDC in Release R052 and R053 and especially the layout of the HV outputs. An internal controller measures the output voltage and regulates it to the nominal value entered by the user or set as default value within the device. Hereby the voltage measurement is always a relative measurement. The output polarity is defined by determine one of the outputs as reference potential (e.g. by termination to ground). Voltage measurement and regulating is also only respecting the relative output voltage of the single HV module in case of a floating operation. The absolute output voltage (as result of output voltage and reference voltage) is not determined by the device. Figure 3 also shows the internal load and measuring resistors.

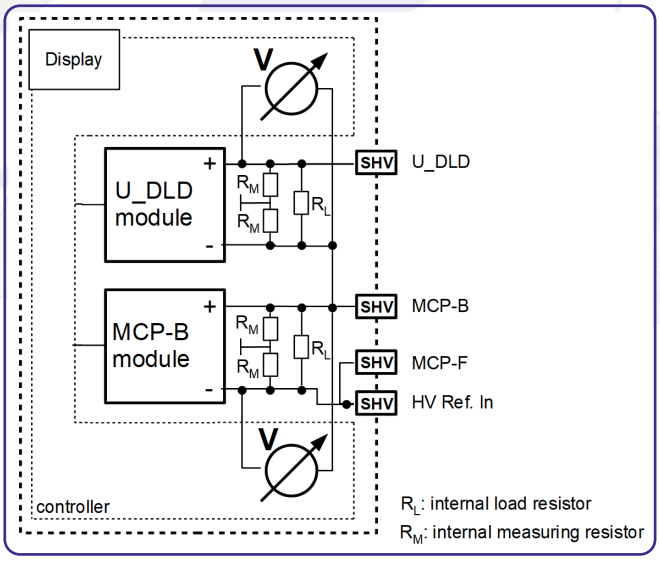

Figure 3: Schematic layout of the HVPS section of R052 and R053 of the Quad Channel USB3.0-TDC showing also the internal load and measuring resistors.

Note

The HVPS section is not producing any output voltage if the reference input "HV Ref. In" is not terminated (either to ground or to an external HV potential), because the HV modules always need to be connected to a reference potential. A SHV termination plug is part of the delivery to terminate the "HV Ref. In" input to ground.

4.3 Layout of the Quad Channel USB3.0-TDC

Figure 4a: Layout of the Quad Channel USB3.0-TDC R053 (similar for R042, R044 and R052, but with reduced numbers of inputs and outputs, see below)

Figure 4b: Layout of the Quad Channel USB3.0-TDC R043.

1. BNC socket for Tag Input (R044, R053)
2. BNC socket for State Input (R044, R053)
3. BNC socket for Master Reset Input (R044, R053)
4. BNC sockets for ADC - Input and ADC + Input (R044, R053)
5. HDMI Socket for DLD Readout Cable from ACU with M3 Thread for Strain Relief (R042, R043, R044, R052, R053)
6. BNC Sockets for external Start Input and Output (R042, R043, R044, R052, R053)
7. BNC Sockets for Device Synchronization Signal IN and OUT (R042, R043, R044, R052, R053)
8. USB Connection Socket (R042, R043, R044, R052, R053)
9. SHV Connector for Input of external Reference Potential (max. +/-1,000V). Check with your MCP or DLD Manual for details on maximum Reference Potential (R052, R053)
10. SHV Connector for Output of Reference Potential to Front Side of MCP Stack within a MCP or Delayline Detector (R052, R053)
11. SHV Connector for Output of Operation Voltage for the MCP stack within a MCP or Delayline Detector (R052, R053)
12. SHV Connector for Output of Operation Voltage for the Detector Anode (R052, R053)
13. BNC Connector for Hardware Interlock; output of BNC Connector must be grounded to deactivate Interlock (R052, R053)
14. Device Ground Connection (R042, R044, R052, R053)

15. Ethernet Connection for remote control of HVPS section (R052, R053)
16. Power Socket (R042, R043, R044, R052, R053)
17. Power Switch to turn the TDC ON/OFF. Lighted, when set to ON (R042, R043, R044, R052, R053)
18. Hardware Reset Button (R052, R053)
19. Status LEDs for Power (lightens up when device is switched on) and Ethernet Connection (lightens up only when a software is connected to the HV Supply) (R052, R053)
20. Touch Display (R052, R053)
21. Control Knob for High Voltage Adjustment (R052, R053)
22. Control Knob for Channel Selection (R052, R053)

4.3.1 TDC Stop Inputs

The Quad Channel USB3.0-TDC provides a HDMI socket for the 4 signal inputs (stop inputs) from the ACU. The TDC inputs are laid out for PECL levels.

4.3.2 TDC Start Input

An external start signal must be provided to the TDC for real time resolved measurements. The external start signal must be applied as a LVTTL (minimum amplitude of at least +2.1V on 50Ohms) signal to the "TTL START" input (BNC socket) for R012, R013 and R022 and as NIM signal to the "Start Input" (LEMO 00 socket) for R042. In addition the software must be set to accept external start signals, by changing the corresponding entry in the tdc_gpx3.ini file.

The corresponding entry in the tdc_gpx3.ini file is:

Ext_Gpx_Start = X

X is either NO or YES. **The default setting is YES**.
"Ext_Gpx_Start" = YES must be set for the TDC to accept the external start signal.
In addition the following entries in the tdc_gpx3.ini must be set as follows:

StartCounter = YES
StartPeriod = 0x800000

Measurements are performed in respect to an internal start signal of the TDC when "Ext_Gpx_Start" = NO. This internal start signal has no time correlation to any external clock and therefore also not to the incoming stops. It can be used for pure 2D(x, y) measurements.
Any external start signal must be disconnected from the start input of the TDC, when working with the internal start signal.

The rise time of the start signal is of great importance, the faster the rise time, the better the time resolution. The maximum frequency of the start pulse must not exceed 9MHz.

Note

Do not forget to save the inifile after any changes you make and restart the software. For further information check the software manual.

Note

Take care that measurements are performed either with the internal start signal (Ext_Gpx_Start = 0 respectively = NO) and no signal applied to the TTL Start Input (BNC socket) or with an external start signal (Ext_Gpx_Start = 1 respectively = YES) applied to the TTL Start Input. In all other cases the TDC is not working correctly.

The start input of the TDC cannot handle pulses which are arriving in a time interval of smaller than 120ns (e.g. as produced by connecting/ disconnecting the start signal during TDC operation). If two such subsequent pulses are applied to the start input of the TDC, the device will still deliver results, but these results might contain wrong timing information.

The TDC does also not work with start signals of frequencies larger than 9MHz. For this reason, the TDCs are equipped with an internal frequency divider. Larger start pulse frequencies must be divided down by an appropriate dividing factor (e.g. dividing factor of 16 for 80MHz start pulse frequency). For start frequencies smaller then 25kHz the user must make sure that all stop signals are provided within a time window of 40µs after each start. Otherwise the TDC will deliver wrong time results, which are not easy to be identified as such.

Note

The temporal resolution is influenced mainly by the quality of the start signal because the TDC measures the time of a rising or a falling edge using a constant voltage threshold. Lower precision than expected may be observed for slow rise or fall times of the signals or in case of any ripple/jitter on the switching edge of the signals. Therefore, if the signals are varying in amplitude, one needs to process them by external electronics components (e.g. constant fraction discriminators, CFDs).

4.3.3 TDC Start Output

The TDC holds an internal electronics, which provide the TDC start signal for further extended measurement use. The "TTL START OUT" (BNC socket) provides either the external start if applied or the internal start, generated by the FPGA.

4.3.4 Device Synchronization Signal IN/OUT

The data acquisition can be synchronized to an external signal for various measurement application linked to external devices. This device synchronization signal has to be applied as LVTTL signal to the "SYNC IN" (BNC socket) of the TDC. This functionality is switched on/off within the tdc_gpx3.ini file.

The corresponding entry in the tdc_gpx3.ini file is:

Ext_trigger = X

X is either NO or YES. **The default setting is NO**.
The TDC ignores any external synchronization signals if "Ext_trigger" = NO. In case that "Ext_trigger" = YES and the "SYNC IN" signal is not provided, the device will not come to operation at all.

The TDC provides always a LVTTL signal on the "SYNC OUT" (BNC socket) after the end of each acquisition, independent on the setting of "Ext_trigger".

Note

Do not forget to save the ini file after any changes you make and restart the software. For further information check the software manual.

4.3.5 Start Frequency Divider

The maximum start frequency of the Quad Channel USB3.0-TDC devices is 9MHz. To cope with larger start frequencies the TDCs are equipped with an internal start frequency divider for external start frequencies of up to 150MHz (this mode only works when using the external start input). Herewith the frequency divider can operate with different dividing factors, which can be set within the software, to always guarantee a start frequency of below 9MHz.
The frequency divider is switched on/off within the tdc_gpx3.ini file, in which also the dividing factors are set.
The corresponding entry in the tdc_gpx3.ini file is:

Start_Divider = X

X is an integer value and must be one of the following values: 0, 2, 4, 8, 16 or 32. The value 1 is not allowed.
The default setting is 0
X = 0 switches off the start divider and leads to normal operation without dividing the start frequency.

The time histogram will appear X times in series, when using a dividing factor of X. This is due to the fact that only each 1st start pulse out of a sequence of X start pulses will be accepted as start signal, while all stop signals are detected. This leads to the multiple time histograms that appear sequentially in time. The multiple histograms can be resorted to one single time histogram by a MODULO-operation during data analysis.

4.3.6 Tag Signal Input

The tag input is an additional counter input for signal counting. The counter number is included into the general data stream of the TDC. The tag signal has to be applied as a LVTTL (low voltage TTL) signal on 50Ohms to the "TAG IN" (BNC socket) of the TDC.
In addition changes in the tdc_gpx3.ini file must be made for the tag signal to be registered by the TDC.

The corresponding entry in the tdc_gpx3.ini file is:

TimeTag = X

X is an integer value and must be one of the following values: 0, 1, 2, 3, 4, 5 or 6.
The default setting is 0.
Each value represents a certain functionality, which is described below:

TimeTag = 0 ;tag counting is switched off and any signal to the "TAG IN" is ignored, nBytes can be set to 4 or 8 (see below for further details on nBytes). Also any state input, master reset input or ADC input signals are ignored.

TimeTag = 1 ;the tag is counting the internal 80MHz clock signal of the FPGA and is therefore functioning as a timer. Any signal to the "TAG IN" is ignored. This mode is not working in combination with the state input.

TimeTag = 2 ;the tag is counting the external LVTTL signal applied to the "TAG IN". The counter is reset with the start of a new measurement. This mode is not working in combination with the state input.

TimeTag = 3 ;tag counting is switched off and any signal to the "TAG IN" is ignored. This value must be set for using the ADC functionality in combination with the state input and the master reset input.

TimeTag = 4 ;corresponds to the setting of TimeTag = 3.

TimeTag = 5 ;must be set for using the tag as timer (similar to TimeTag = 1) but in combination with the state input. A pulse on "Tag In" resets the timer to 0.

TimeTag = 6 ;must be set for using the tag as counter (similar to TimeTag = 2) but in combination with the state input.

The number of bits which are available for each detector event (x, y, t) is defined by an additional parameter called "nBytes" in the tdc_gpx3.ini file.

The corresponding entry in the tdc_gpx3.ini file is:

nBytes = X

X is an integer value of either 4 or 8. **The default setting is 8**.

Different settings of "nByte" parameter in combination with different settings of the "TimeTag" parameter results in a further differentiation of the TimeTag functionality as described below:

"nBytes" = 4 ;each detector event x, y, t has a length of 32bit. The sub-definition for the different coordinates x, y and t is defined by the "DataFormat" (e.g. "DataFormat" = 2 ;x = 11bit, y = 11bit, t = 10bit, see the software manual for further details).

"nBytes" = 8
"TimeTag" = 0 ;each detector event x, y, t has a length of 64bit. The sub-definition for the different coordinates x, y and t is defined by the "DataFormat" (e.g. "DataFormat" = 2 ;x = 11bit, y = 11bit, t = 42bit, see the software manual for further details).

"nBytes" = 8
"TimeTag" > 0 ;each detector event x, y, t has a length of 64bit. The first 32bit are used for the tag counter. The second 32bit are sub-definition for the different coordinates x, y and t is defined by the "DataFormat".
In case that "TimeTag" > 0, "nBytes" is set to 8 automatically within the software and any ini file settings are ignored.

4.3.7 Master Reset Input

The master reset input is treated as an additional sign signal within the TDC and is counted up in a software counter within the dll.
In addition the master reset input is connected to the reset pin of the TDC chip. Each time a signal is applied to the master reset input the corresponding software counter is counting up and the input and output FIFOs of the TDC chip are cleared (all old TDC data are erased).
A LVTTL (low voltage TTL) signal on 50Ohms has to be applied to the "MASTER RESET IN" BNC socket of the TDC.

4.3.8 State Signal Input

The state signal has to be applied as a LVTTL (low voltage TTL) signal on 50Ohms to the "STATE IN" (BNC socket) of the TDC.
In addition, the value of the variable named "TimeTag" in the tdc_gpx3.ini file (depending on the software version which is used) must be adapted for the state signal to be registered by the TDC.
The state signal input assumes values 0 or 1, depending on the given electronic level of the LVTTL signal (low or high).
For the state/sign input to be functioning the following variables in the tdc_gpx3.ini must be used:

TimeTag = 3 ;must be set for using the state input in combination with the ADC functionality and the master reset input. The tag counting is switched off and any signal to the "TAG IN" is ignored.

TimeTag = 4 ;corresponds to the setting of TimeTag = 3

TimeTag = 5 ;must be set for using the state/sign input. Hereby the state input functions in combination with the tag signal functioning as a timer, counting the internal 80MHz clock signal of the FPGA. A signal on "TAG IN" resets the timer to 0.

TimeTag = 6 ;must be set for using the state input. Hereby the state/sign input functions in combination with the tag signal functioning as a counter, counting the external LVTTL signal applied to the "TAG IN".

4.3.9 ADC Input

The Quad Channel USB3.0-TDC R044 comes with an integrated 14bit Analog-to-Digital converter with a differential signal input ("ADC IN +" and "ADC IN -") which is laid out for analog voltages between +10V and -10V.
To work with the ADC the value of the variable named "TimeTag" in the tdc_gpx3.ini file must be adapted in the following way:

TimeTag = 3 ;must be set for using the ADC functionality. This will work also in combination with the state input and the master reset input. The tag counting is switched off and any signal to the "TAG IN" is ignored.

TimeTag = 4 ;corresponds to the setting of TimeTag = 3

In case that no differential analogue signal would be available, one can also use a single non-differential signal. In this case one has to use the positive input ("ADC IN +") of the ADC, while terminating the negative input ("ADC IN -") to ground. Please be aware that this way of operating is working, but it is more prone to noise.

4.4 Operation of the HVPS Section (R052, R053)

After switching on the TDC, the display shows the "Surface Concept" animated logo, while the device is scanning for internal available HV modules and their specific settings. This can take up to several seconds. If the device is ready for operation, it switches into the standby mode and shows an empty mask for the voltage adjustment (see **Figure 5**).

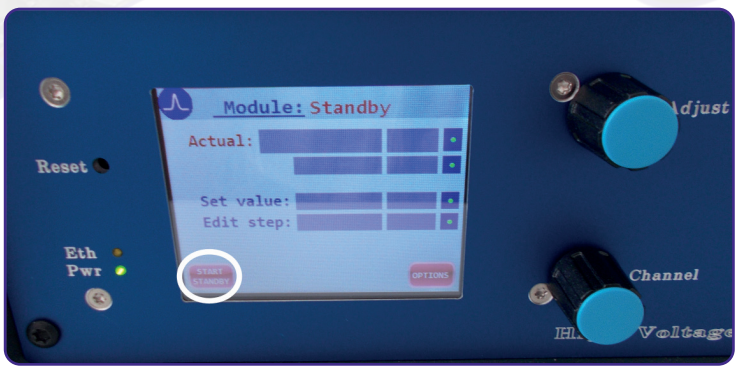

Figure 5: Standby mode.

Push the "Start/Standby" button in the lower left corner of the display to switch on the high voltage.
Alternatively one can press the "Channel" control knob.

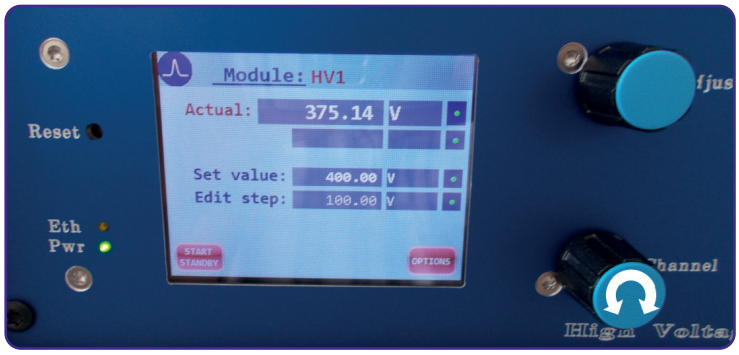

Figure 6: Operation mode.

After switching on the high voltage the device is in the so called operation mode. In operation mode the display shows the name of the selected channel in the top line (in this case "HV 1") as well as the output voltage of that channel.
The different HV channels can be selected by turning the "Channel" control knob.

Figure 7: Operation mode – voltage adjustment.

The "Adjust" control knob is used to adjust the output voltage.
Turn the "Adjust" control knob clockwise/counterclockwise to increase/decrease the value of the output voltage in a step width as defined in the line "edit step".

The line "set value" displays the nominal value for the output voltage as adjusted by the user. Voltage adjustment can only be made in this line.

The line "actual" displays the actual value for the output voltage on the output connector as measured by the device.
The device always regulates the actual value of the output voltage to fit to the nominal value as set by the user.
Hereby the voltage measurement is always a relative measurement between the two HV outputs of one channel. Additional reference voltages (e.g. in floating operation) are not measured and therefore are also not displayed (see **Chapter 4.4.1** for further details)

Turn the "Adjust" control knob clockwise/counter-clockwise while pushing it to increase/decrease the step width in the line "edit step".
Turn the "Adjust" control knob clockwise/counter-clockwise while pushing it to move the cursor position to the right/left.

Push the "Start/Standby"-button in the lower left corner of the display again to switch back to the "Standby" mode.

4.4.1 Operation of a Delayline Detector with the R052, R053

The HVPS section of the R052, R053 is specified for the operation with an external reference voltage of maximum +/-1,000V. Higher voltages can lead to internal HV sparking and to a damage of the device.
Please also respect the corresponding specifications for the maximum voltage for the MCP front potential of your MCP or delayline detector (see the manual and the specification sheet of your MCP/delayline detector for further details).

In some cases a delayline detector is operated with the front side of the MCP stack terminated to ground. But for many other applications it is necessary to apply some external reference voltage to the front side. In this case the floating capability of the HVPS D allows a more insusceptible supply of the correct detector operation voltage because the external reference voltage must not be taken into account for the DLD operation voltage. Additionally this wiring also saves the detector intrinsically from any over-voltage in case of a sudden drop of the external reference voltage.
In general there are three different application cases concerning reference potential to the front side of the detector's MCP stack.

For example: Assume an operation voltage of a detector of +1,900V.
Application case 1: The detector should be operated with the MCP front side connected to ground. In this case the SHV termination plug is connected to the "HV Ref. In" input. "MCP-B" is set to the detectors operation voltage. The display shows a value of MCP-B = 1,900V and U_DLD = 400V. The output voltage in respect to the ground potential is MCP-B = +1,900V and U_DLD = + 2,300V.

Application case 2: The detector should be operated with the MCP front side connected to +1,000V. In this case the external reference voltage is connected to the "HV Ref. In" input. First set the HVPS D to the detectors operation voltage. Then increase the external reference voltage to the +1,000V. The display shows a value of MCP-B = 1,900V and U_DLD = 400V, but the output voltage in respect to the ground potential is MCP-B = +2,900V and U_DLD = +3,300V.

Application case 3: The detector should be operated with the MCP front side connected to -500V. In this case the external reference voltage is connected to the "HV Ref. In" input. First set the HVPS D to the detectors operation voltage. Then increase the external reference voltage to the -500V. The display shows a value of MCP-B = 1,900V and U_DLD = 400V, but the output voltage in respect to the ground potential is MCP-B = +1,400V and U_DLD = +1,800V.


This side has been left blank on purpose.

5 Additional Menu Settings

Pressing the "Option" button in the lower right corner of the device display, the device will switch to the overview display of the additional device options. The available options are device depending. Press the "Exit" button to switch back to the display of the operation voltages.

Figure 8: "Device Options" sub-menu.

The overview of the device options show the different available options like the contact page for surface concept or special device specific functions.
Open the specific sub-menu by pressing the corresponding button in the touch display.

5.1 Special Function Check

The sub-menu "Special Function Check" in the device options display the different special functions currently available for the Surface Concept HVPS D Series.
Not all listed functions are available for each single device layout.

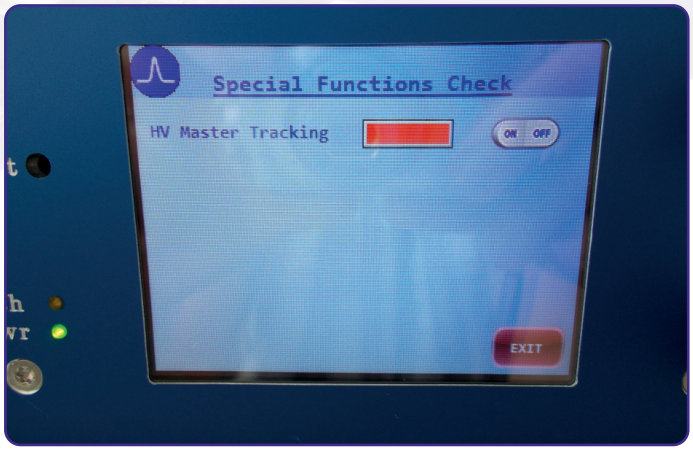

Figure 9: "Special Functions Check" sub-menu.

The "HV Master Tracking" allows the HVPS to track an external reference voltage and to produce an output voltage which is in a fixed defined relation to the master voltage.
Please note: This function differs from the floating functionality, because the master voltage is "only" measured within the device and the HVPS is producing a corresponding output voltage.

The "HV Master Tracking" can be switched ON/OFF by clicking on the corresponding button on the display (not available for the R052, R053).

5.2 Contact Surface Concept

The sub-menu "Contact Surface Concept" in the device options displays the Surface Concept contact information. Press the "Exit" button to leave this sub-menu.

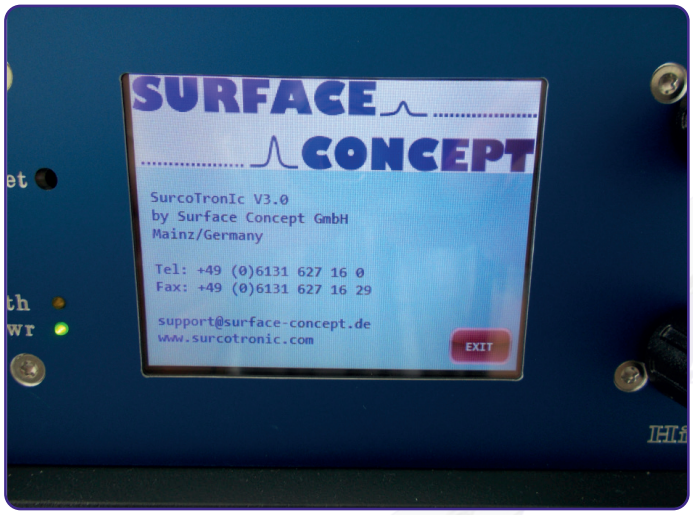

Figure 10: "Contact Surface Concept" sub-menu.

Error states of the device are indicated by error messages in the display.

Figure 11: Error code – Interlock.

Err – Interlock

The device interlock is active and is blocking the HV output. Please terminate the interlock to ground using either the BNC termination plug (part of the delivery) or check the proper functionality of the use device which is providing the interlock.

6 Technical Data

Quad Channel USB3.0-TDC 04R - Release 042 & 043:

- 19“ 3HE Rack Mount Housing (R042)
- 2HE table top housing with 254mm x 272mm x 106mm (w/d/h) (R043)
- Number of Stop Inputs: 4
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 27.4ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels
- Trigger to rising edge
- Start retrigger rate (max): 9MHz
- Measurement range: 0 ns – 40µs in start-stop operation
  (measurement range of 40µs corresponds to a start frequency of 25kHz)
- Internal start frequency divider (2-, 4-, 8-, 16- and 32-fold divider)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 80MHz internal device measurement rate
- Stop Signal Input: Low voltage PECL (differential signal) on differential multiline connector (adapted to connector layout of ACU of the detector head)
- External Start Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Output: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- USB Interface for Data Transfer

Quad Channel USB3.0-TDC 04R - Release 044:

- 19“ 3HE Rack Mount Housing
- Number of Stop Inputs: 4
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 27.4ps

- 5.5ns pulse-pair resolution on one channel and 0ns between two channelsTrigger to rising edge
- Start retrigger rate (max): 9MHz
- Measurement range: 0 ns – 40µs in start-stop operation
  (measurement range of 40µs corresponds to a start frequency of 25kHz)
- Internal start frequency divider (2-, 4-, 8-, 16- and 32-fold divider)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 80MHz internal device measurement rate
- Stop Signal Input: Low voltage PECL (differential signal) on differential multiline connector (adapted to connector layout of ACU of the detector head)
- External Start Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Output: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- USB Interface for Data Transfer

Quad Channel USB3.0-TDC 04R - Release 052:

- 19“ 3HE Rack Mount Housing
- Number of Stop Inputs: 4
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 27.4ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels
- Trigger to rising edge
- Start retrigger rate (max): 9MHz
- Measurement range: 0 ns – 40µs in start-stop operation
  (measurement range of 40µs corresponds to a start frequency of 25kHz)
- Internal start frequency divider (2-, 4-, 8-, 16- and 32-fold divider)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 80MHz internal device measurement rate
- Stop Signal Input: Low voltage PECL (differential signal) on differential multiline connector (adapted to connector layout of ACU of the detector head)

- External Start Signal Output: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- Number HV Output Channels: 2
- HV Output Connector: SHV5
- Output Voltage Range (channel U_DLD): 0, 50V - 400V
- Output Voltage Range (channel MCP-B): see specification sheet
- Output Polarity: see specification sheet
- Input Connector for Reference Input: SHV5
- Maximum Voltage for external Reference Potential: +/- 1000V
- USB Interface for Data Transfer of TDC Data
- Ethernet Interface for Remote Control of HVPS

Quad Channel USB3.0-TDC 04R - Release 053:

- 19“ 3HE Rack Mount Housing
- Number of Stop Inputs: 4
- Number of Start Inputs: 1 (common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- Digital time bin resolution per channel: 27.4ps
- 5.5ns pulse-pair resolution on one channel and 0ns between two channels
- Trigger to rising edge
- Start retrigger rate (max): 9MHz
- Measurement range: 0 ns – 40µs in start-stop operation
  (measurement range of 40µs corresponds to a start frequency of 25kHz)
- Dynamic range: 2E19
- All channels provide precisely an equal resolution
- 32-fold multi-hit capability per channel
- 80MHz internal device measurement rate
- Stop Signal Input: Low voltage PECL (differential signal) on differential multiline connector (adapted to connector layout of ACU of the detector head)
- External Start Signal Input: Low voltage TTL on 50Ohm BNC socket
- External Start Signal Output: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Input: Low voltage TTL on 50Ohm BNC socket
- Device Synchronization Signal Output: Low voltage TTL on 50Ohm BNC socket
- Tag, State and Master Reset Input: Low voltage TTL on 50Ohm BNC socket
- ADC Input: 14bit ADC with differential analog signal input (+/-10V) on BNC sockets
- Output Voltage Range (Channel MCP-B): see specification sheet

- Number of HV Output Channels: 2
- HV Output Connector: SHV5
- Output Voltage Range (Channel U_DLD): 0, 50V - 400V
- Output Polarity: see specification sheet
- Input Connector for Reference Input: SHV5
- Maximum Voltage for external Reference Potential: +/- 1000V
- USB Interface for Data Transfer of TDC Data
- Ethernet Interface for Remote Control of HVPS

Line Input

Electrical Input (LINE)	85 V – 260 V, 50/60 Hz
Power	65 Watt (max.)
Fuse	1x T 1.6 A

7 List of Figure

EC Declaration of Conformity

Manufacturer

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Germany

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Product
Model No.

Time Measurement System - TDC
Quad Channel USB 3.0-TDC 04R
(as part of the Delayline Detector Package)

The above named products comply with the following European directive:

89/336/EEC	Electromagnetic Compatibility Directive, amended by 91/263/ EEC and 92/31/ EEC and 93/68/EEC
73/23/EEC	Low Voltage Equipment Directive, amended by 93/68/EEC

The compliance of the above named product to which this declaration relates is in conformity with the following standards or other normative documents where relevant:

EN 61000-6-2:2005+AC:2005	Electromagnetic compatibility (EMC): Generic standards - Immunity for industrial environments
EN 61000-6-4:2007+A1:2011	Electromagnetic compatibility (EMC): Generic standards - Emission standard for industrial environments
EN 61010-1: 2010	Safety Requirements for Electrical Equipment for Measurement, Control and Laboratory Use

For and on behalf of **Surface Concept GmbH**

Mainz,……01.12.2019…… (Date)

Legal Signature…… (Dr. Andreas Oelsner)

This declaration does not represent a commitment to features or capabilities of the instrument. The safety notes and regulations given in the product related documentation must be observed at all times.